530,848

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 April 2004 (22.04.2004)

PCT

(10) International Publication Number
WO 2004/033769 A1

(51) International Patent Classification[7]: C30B 28/02, H01L 31/18, 21/20

(21) International Application Number: PCT/AU2003/001313

(22) International Filing Date: 7 October 2003 (07.10.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2002951838 8 October 2002 (08.10.2002) AU

(71) Applicant *(for all designated States except US)*: **UNISEARCH LIMITED** [AU/AU]; Rupert Myers Building, Level 2, Gate 14, Barker Street, UNSW, Sydney, NSW 2052 (AU).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ABERLE, Armin** [DE/AU]; 8/4 Fabry Street, Botany, NSW 2019 (AU). **WIDENBORG, Per** [SE/AU]; Centre for Photovoltaic Engineering, The University of NSW, Sydney, NSW 2052 (AU). **STRAUB, Axel** [DE/AU]; Centre for Photovoltaic Engineering, The University of NSW, Sydney, NSW 2052 (AU). **NEUHAUS, Dirk-Holger** [DE/DE]; Centre for Photovoltaic Engineering, The University of NSW, Sydney, NSW 2052 (AU). **HARTLEY, Oliver** [DE/GB]; Flat 13 The Anglers, 59-61 High Street, Kingston upon Thames KT1 1NB (GB). **HARDER, Nils-Peter** [DE/DE]; Centre for Photovoltaic Engineering, The University of New South Wales, Sydney, N.S.W. 2052 (AU).

(74) Agent: **F B RICE & CO**; 605 Darling Street, Balmain, NSW 2041 (AU).

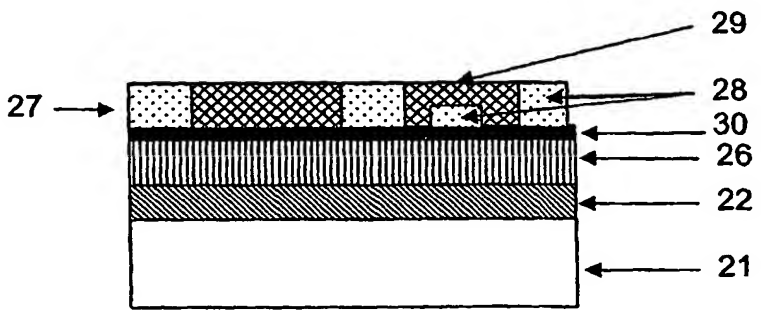
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: FABRICATION METHOD FOR CRYSTALLINE SEMICONDUCTOR FILMS ON FOREIGN SUBSTRATES



(57) Abstract: The invention provides a method of forming a polycrystalline semiconductor film (26) on a supporting substrate (21, 22) of foreign material. The method involves depositing a metal film (23) onto the substrate, forming a film of metal oxide and/or hydroxide (24) on a surface of the metal, and forming a layer of an amorphous semiconductor material (25) over a surface of the metal oxide and/or hydroxide film. The entire sample is then heated to a temperature at which the semiconductor layer is absorbed into the metal layer and deposited as a polycrystalline layer (26) onto the target surface by metal-induced crystallisation. The metal is left as an overlayer (27) covering the deposited polycrystalline layer, with semiconductor inclusions (28) in the metal layer (29). The polycrystalline semiconductor film (26) and the overlayer (27) are separated by a porous interfacial metal oxide and/or hydroxide film (30). The metal in the overlayer and the interfacial metal oxide and/or hydroxide film are then removed with an etch which underetches the semiconductor inclusions to form freestanding islands. Finally the freestanding semiconductor "islands" are removed from the surface of the polycrystalline semiconductor layer by a lift-off process. There is also provided a method for the formation of a further polycrystalline layer using a polycrystalline layer as a seed layer. The seed layer may be a polycrystalline semiconductor layer formed by the metal induced crystallisation method. The surface of the seed layer is first cleaned to remove any oxides or other contaminants, before forming an amorphous layer of a semiconductor material over the cleaned surface of the seed layer, and heating the substrate, the seed layer and the amorphous layer to crystallise the semiconductor material by solid phase epitaxy.

WO 2004/033769 A1